REMARKS

Claims 1-22 are currently pending in connection with the present application. Claims 1, 7, 13, 17, 21 and 22 are independent claims. By this amendment, claims 1, 2, 7, 8, 13, 14, 17 and 18 have been amended. Minor amendments were made to the claims to overcome the claims rejections under 35 U.S.C. §112, second paragraph. Support for these amendments may be found on paragraph [0029] and [0030] of the specification. There is no new matter. Applicants traverse the rejection set forth in the Office Action dated February 14, 2006.

Priority Documents

Applicants acknowledge and thank the Examiner for the acknowledgement of priority under 35 U.S.C. §119, and further thank the Examiner for the acknowledgement of receipt of all the necessary priority documents as shown in the Office Action dated February 14, 2006.

Information Disclosure Statement

Applicants acknowledge and thank the Examiner for the careful consideration of all of the references listed in the information disclosure statement filed July 7, 2005.

Drawings

Applicants acknowledge that the Drawings filed on April 2, 2004 have been accepted.

ALLOWABLE SUBJECT MATTER

Absent an indication otherwise, Applicant assumes that claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the features of the base claim and any intervening claims. However, it is submitted that claims 1-5 and 7-20 are allowable in view of the following remarks and amendments.

35 U.S.C. §112, SECOND PARAGRAPH REJECTIONS

Claims 4, 7-12 and 16-22 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as his invention. Applicant respectfully traverses this rejection.

With respect to claim 4, Applicant submits that "a power down signal" recited in line 2 is clearly an additional limitation to the gate circuit in claim 1. Applicant has clearly recited "a power down signal" to indicate this as a new limitation. Applicant further submits that in claim 4, the "output driving signal" depends on both a precharging control signal and a power down signal, whereas in claim 1, the output driving signal depends on the precharging control signal. Accordingly, Applicant requests that the rejection of claim 4 be withdrawn. For somewhat similar reasons, Applicant submits that the rejections of claims 10, 16 and 20 should also be withdrawn.

With respect to claims 7 and 17, Applicant has amended claim 7 and 17 to account for the lack of antecedent basis for the terms "the second output driver" and "a first data bit" in claims 7 and 17, respectively. Accordingly, Applicant requests that the rejection of claims 7 and 17 be withdrawn.

With respect to claims 21 and 22, Applicant submits that these claims are clearly directed to "a method." The claims rejected in *Ex parte Lyell*, cited by the examiner, were directed to "a system and method" and included both method steps and system components in the body of the claims.[1] In contrast, independent claims 21 and 22 are clearly distinguished from those rejected in *ex parte Lyell*, because independent claims 21 and 22 recite various components in the preamble which are used to perform the claimed method, thereby limiting the claims and not

[1] *Ex parte Lyell*, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990).

adding ambiguity. Therefore, Applicant requests the rejection of claims 21 and 22 be withdrawn.

Accordingly, Applicant requests that the rejection of claims 4, 7-12 and 16-22 under 35 U.S.C. §112 be withdrawn.

DESCRIPTION OF AN EXAMPLE EMBODIMENT

An example embodiment of the present invention is directed to a method and system for decreasing transmission timing variations, particularly in circuits using high-speed data transmission requiring reliability and stability. As timing variations deteriorate in a circuit, the effective window in which data may be transferred narrows. This makes it more difficult to accurately receive data. This variation is caused by the distance between the transmitting and receiving circuit, because of the time necessary for the transmitting medium to obtain a readable logical state (e.g., "0" or "1"). FIG. 4 illustrates a data transmission pattern associated with a first data bit that has been transmitted over a precharged data channel. Prior to transmitting a first bit on a data channel, the data channel may be precharged with a voltage level Vp during a waiting time, before the first bit is transmitted to the data channel (e.g., if a power voltage is high at 1.8V, a precharged voltage Vp may be set approximately to 1.4V). The time for precharging the data channel may comprise one-half to one period of a system clock cycle before the first bit is transmitted.

PRIOR ART REJECTIONS

35 U.S.C. §102(b) Yau Rejection

Claims 1-5, 13-16 and 21 stand rejected under 35 U.S.C. §102(b) as being anticipated by Yau et al. (U.S. Patent No. 6,498,520). Applicants respectfully traverse this rejection.

Yau is directed at a system for minimizing the effect of clock skew. A global bit value from the global bit channel (gbit) is provided as input to a circuit which uses a clock signal, a select signal and the global bit value to minimize the effects of the clock skew on the global bit channel. The global bit value is processed along side the clock and select signals to provide a realigned logical state signal, thereby minimizing the effect of the clock skew in the global bit channel.

Applicant submits that Yau fails to teach or suggest "a gate circuit for inputting a precharging control signal and for generating an output driving signal in response to the precharging control signal before a data bit is input; and an input driver connected to a data channel and responsive to the output driving signal for precharging the data channel to a voltage level before the data bit is input," as recited in independent claim 1.

On the contrary, Yau teaches responding to a global bit value on the global bit channel by using a select signal and a clock value to minimize the clock skew on the global bit channel. Yau requires the global bit value as input which clearly shows that Yau cannot teach, suggest or render obvious at least "generating an output driving signal ... before a data bit is input" or "an output driver responsive to the output driving signal for precharging a data channel to a voltage level before the data bit is input," because Yau responds and corrects for the clock skew using an input data bit (i.e., the global bit value).

Accordingly, Applicant respectfully submits that Yau fails to disclose, teach, suggest, or render obvious each and every feature of independent claim 1 and claim 1 is therefore patentable. For somewhat similar reasons, independent claims 13 and 21 are also patentable (although claims 1, 13 and 21 should be interpreted solely based upon the limitations set forth therein). Therefore, Applicant respectfully requests that the rejection of independent claims 1, 13 and 21, and dependent claims 2-5 and 14-16, under 35 U.S.C. §102(b), be withdrawn.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-22 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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